AMENDMENT TO CLAIMS

The following listing of claims replaces all prior listings of claims in the application:

1. (Original) A memory comprising:
at least one data storage area comprising a plurality of data storage locations;
an access circuitry for accessing the data storage locations for retrieving or altering a data content thereof; and
at least one first user-configurable flag element and a second user-configurable flag element associated with said storage area, the first and second flag elements being used to define a protected state of the data storage area against alteration of the content of the data storage locations thereof, the protected state defined by the at least one first flag element being user-removable, while the protected state defined by the second flag element being permanent and non-removable.

2. (Currently Amended) The memory of claim ~~1~~3, in which said second flag element can be set to define the permanent protected state of the respective data storage area irrespective of the fact that the at least one first flag element is set to define the removable protected state.

3. (Previously Presented) A memory comprising:
at least one data storage area comprising a plurality of data storage locations;
an access circuitry for accessing the data storage locations for retrieving or altering a data content thereof; and
at least one first user-configurable flag element and a second user-configurable flag element associated with said storage area, the first and second flag elements being used to define a protected state of the data storage area against alteration of the content of the data storage locations thereof, the protected state defined by the at least one first flag element being user-

removable, while the protected state defined by the second flag element being permanent and non-removable,

in which the at least one first flag element has a first state and a second state, in which any alteration of the data content of the respective data storage area is allowed and, respectively, inhibited, and

the second flag element has a first state and a second state, in which changing of the state of the first flag element from the second state to the first state is allowed and, respectively, inhibited, so that when the second flag element is in the second state the respective data storage area is permanently protected against alteration of the data content thereof.

4. (Currently Amended) The memory of claim ~~1~~3, in which the at least one first flag element comprises a non-volatile programmable and erasable storage element, and the second flag element comprises a one-time programmable non-volatile storage element.

5. (Original) The memory of claim 3, in which the second flag element can be set into the second state only if the at least one first flag element is in the second state.

6. (Currently Amended) The memory of claim ~~1~~3, in which said at least one storage area comprises at least two storage areas, and in which for each of said at least two storage areas a respective first and second user-configurable flag elements are provided.

7. (Currently Amended) The memory of claim ~~1~~3, comprising at least one further data storage area comprising a plurality of storage locations, and user-configurable flag means associated with said at least one further data storage area adapted to define a protected state of the at least one further data storage area against the alteration of the content of the respective storage locations, said protected state being removable by the user and not permanent.

8. (Currently Amended) The memory of claim ~~1~~3, comprising means for conditioning the configuring of said first and second flag elements by the user on the recognition of the user by the memory.

9. (Currently Amended) A memory, comprising:

a first data-storage portion operable to store first data;

a first status portion operable to have one of a first state and a second state, ~~corresponding to and operable~~ to allow alteration of the data while in the first state, and to prohibit alteration of the data while in the second state~~indicate first and second states of the first data-storage portion~~; and

a second status portion operable to have one of a third state and a fourth state, to allow the state of the first status portion to be altered while in the third state, and to prohibit the states of the first and second status portions from being altered while in the fourth state~~corresponding to and operable to indicate a third state of the first data-storage portion~~.

10. (Currently Amended) The memory of claim 9 wherein the second status portion is operable to enter the fourth state ~~indicate the third state~~ only while~~en~~ the first status portion has ~~indicates~~ the second state.

11. (Currently Amended) The memory of claim 9 wherein the second status portion is inoperable to enter ~~indicate~~ the fourth~~third~~ state while~~en~~ the first status portion has~~indicates~~ the first state.

12. (Currently Amended) The memory of claim 9, further comprising:

~~-~~ a second data-storage portion ~~in~~operable to store second data ~~be in the third state~~; and

a third status portion operable to have one of the first state and the second state, to allow alteration of the second data while in the first state, and to prohibit alteration of the data while in the second state.

13. (Currently Amended) The memory of claim 9, further comprising:

a second data-storage portion ~~in~~operable to store second data that is always alterable~~be in the second and/or third states~~.

14. (Currently Amended) The memory of claim 9, wherein:

~~-~~ the third state equals the first state; and

the fourth state equals the second ~~comprises a modifiable~~ state.

15. (Currently Amended) The memory of claim 9, wherein:

-the first status portion is in the first state while storing a first value and is in the second state while storing a second value~~comprises a revocable unmodifiable state~~; and

the second status portion is in the third state while storing a third value and is in the fourth state while storing a fourth value.

16. (Currently Amended) The memory of claim 9, wherein:

-the first status portion is in the first state while storing a first value and is in the second state while storing a second value; and

the second status portion is in the third state while storing the first value and is in the fourth state while storing the second value~~third state comprises an irrevocable unmodifiable state~~.

17. (Currently Amended) A method, comprising:

receiving a request to modify a protection state of a-memory sector ~~having a plurality of states; and~~

granting the request if a status memory associated with the memory sector has an unlocked state; and

denying the request if the status memory has a locked state.~~to modify if the sector is in a first state of the plurality, denying the request to modify if the sector is in a second and/or third state of the plurality~~.

18. (Currently Amended) A method, comprising:

receiving a request to unprotect contents of ~~transition~~ a memory sector ~~from a second or third state to a first state; and~~

granting the request if a status memory associated with the memory ~~to transition if the~~ sector is in an unlocked ~~the second~~ state; and~~,~~

denying the request if the status memory is in a locked state ~~to transition if the portion is in the third state~~.

19. (Currently Amended) A method, comprising:

revocably configuring ~~transitioning~~ a memory sector to prohibit alteration of data stored in the memory sector;~~a revocable unmodifiable state~~; and

irrevocably configuring ~~transitioning~~ the memory sector to prohibit alteration of the data ~~an irrevocable unmodifiable state~~ only after revocably configuring~~transitioning~~ the memory sector to prohibit alteration of the data~~the revocable unmodifiable state~~.

20. (Currently Amended) An electronic system, comprising:

a memory ~~device~~, comprising~~,~~:

a first data~~-~~storage portion operable to store data~~;~~,

a first memory portion coupled and corresponding to the first data-storage portion, the first memory portion operable to have one of a first state and a second state, to allow alteration of the data while in the first state, and to prohibit alteration of the data while in the second state, and

a second memory portion coupled to the first memory portion and operable to have one of a third state and a fourth state, to allow the state of the first memory portion to be altered while in the third state, and to prohibit the states of the first and second memory portions to be altered while in the fourth state, and

a controller coupled to the memory.~~a first memory coupled and corresponding to the first portion, the first memory operable to indicate first and second states of the first portion; and~~

~~a second memory coupled to the first memory and corresponding to the first portion, the second memory operable to indicate a third state of the first portion~~.